WHAT IS CLAIMED IS:

1. A pattern synchronous circuit comprising:

branch means for branching parallel signals of n bits inputted from a parallel signal input terminal into two portions,

frame detection means for using one portion of the parallel signals branched by said branch means as input and detecting a frame identification pattern in the parallel signals to output the position information,

first sort means for using the other portion of the parallel signals branched by said branch means as input and sorting the parallel signals according to a low order bit of the frame position information outputted by said frame detection means, and

second sort means for further using outputs of said first sort means as input and again sorting the parallel signals according to all the bits of the frame position information outputted by said frame detection means.

2. The pattern synchronous circuit as defined in claim 1, wherein

said first sort means comprises:

one shift means for using (n/l)-th bit from the first bit of the parallel signals as input and performing shift operations according to a low order bit of the frame position

information outputted by said frame detection means, and

(1-1) sort means for respectively using (n/1) bits in the continuous parallel signals as input and performing sort operations according to a low order bit of the frame position information outputted by said frame detection means.

3. The pattern synchronous circuit as defined in claim 1, wherein

said second sort means comprises:

delay means for using data obtained by sampling said first sort means every m bits as input and delaying signals,

(m-1) sort means for respectively using data obtained by sampling said mutually different first sort means every m bits as input and performing sort operations according to a low order bit of the frame position information outputted by said frame detection means, and

m shift means for respectively using outputs of said delay means and said sort means as input and performing shift operations according to a high order bit of the frame position information outputted by said frame detection means.

4. The pattern synchronous circuit as defined in claim 2 or 3, wherein

said shift means shifts bits without sorting a list of the parallel signals according to the frame position information.

5. The pattern synchronous circuit as defined in claim 2 or 3, wherein

said sort means sorts a list of bits in the same clock of the parallel signals according to the frame position information.

6. The pattern synchronous circuit as in any one of claims 1 to 3, wherein

the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.